M.A.C.H.3

INSTRUCTION MANUAL

MYLSTAR

M.A.C.H. 3 (GAME GV-109)
INSTRUCTION MANUAL

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"WARNING: This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference."

WARNING: The Video Disc Player is to be serviced by an authorized Mylstar Electronics, Inc. distributor onlyl Any attempt to service this unit voids all warranties.

CAUTION: The Video Disc Player must be kept in the horizontal upright position at all times.

When shipping the Video Disc Player to an authorized Mylstar Electronics, Inc. distributor, be certain to replace the shipping screw and bracket and ship in the original box.

Mylstar Electronics, Inc. M.A.C.H. 3 Video Disc Game contains Pioneer LaserDisc™ brand video disc players. LaserDisc™ is a trademark of Pioneer Electronics Corporation and identifies only the video discs and video disc players made by that company.

NOTICE

WARRANTY INFORMATION IS LOCATED ON THE INSIDE BACK COVER.

FOR SERVICE, CALL TOLL FREE: 1-800-323-9121; (ILLINOIS) 1-800-942-1620

I. INSTALLATION

M.A.C.H. 3

MILITARY AIR COMMAND HUNTER

A. SET-UP

1. Unstrap the video disc player from the seat of the player compartment on the SIT-DOWN game or from the main shipping box on the UP-RIGHT game.
2. Open the video disc player box and remove the player by lifting from the front and rear of the unit. Place all cables and the remote control unit in the box and store for future use. These accessories are not used with this game.
3. With the back door open, place the video disc player on the floor in front of the rear cabinet opening with the front of the video disc player facing you.
4. Remove the foam sidings and the plastic bag from the video disc player and store in the video disc players box.

NOTE: All reference to left and right is in relationship to looking into the rear cabinet opening, facing the rear of the CRT.

5. Unravel the video disc player line cord and plug into the outlet labeled VIDEO DISC OUTLET located to the left rear of the video disc platform.

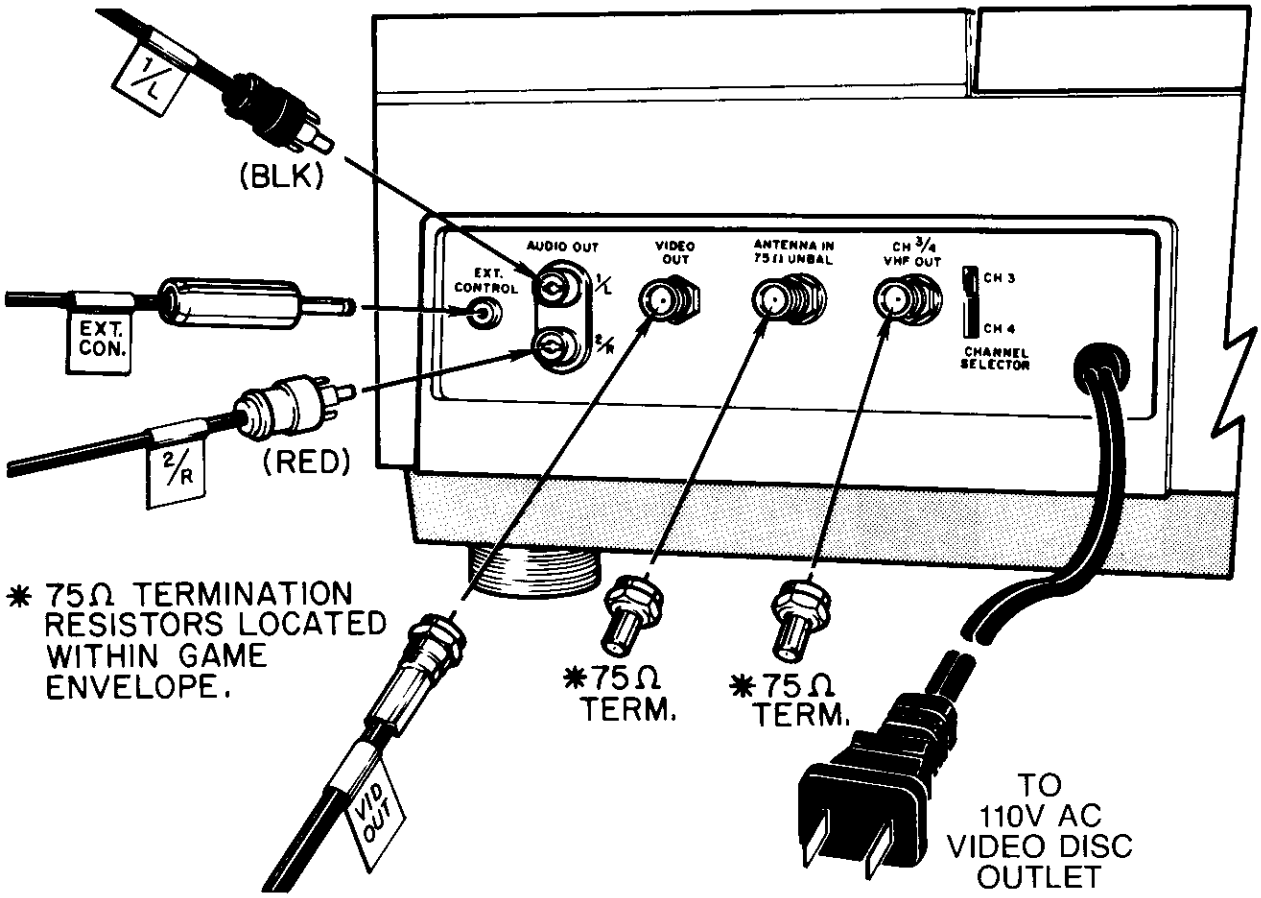
WARNING: Do not plug the video disc player into the CONVENIENCE OUTLET.

6. Be certain the coin door is closed. Plug the game into a 115V AC outlet and turn the game on with the on/off switch located on the lower left back panel.
7. Turn on the video disc player with the on/off switch located on the lower left front panel on the video player unit.
8. Open the top cover of the video disc player by pressing the button labeled REJECT OPEN located directly above the video disc players' power switch. The top will pop up slightly.

WARNING: REMOVE THE SHIPPING SCREW AND BRACKET LOCATED UNDER THE TOP COVER OF THE VIDEO DISC PLAYER IN THE DISC COMPARTMENT WITH A COIN OR SCREWDRIVER BEFORE PLACING THE VIDEO DISC INTO THE DISC COMPARTMENT. Store the screw and bracket in the video disc players' box. REMOVE THE LENS CAP LOCATED TO THE LEFT OF THE SHIPPING SCREW (GREY RUBBER) and store in the disc player box.

9. Remove the video disc from the cardboard shipping sleeve stapled to the right inner wall of the rear cabinet. The cardboard shipping sleeve can be used to mail the video disc to an authorized Mylstar Electronics, Inc. distributor for service. Insert the video disc with the aluminum side up into the disc compartment on the spindle post.
10. Close the top cover being certain it locks down.
11. TURN OFF THE GAME POWER.

I. INSTALLATION



CABLE INSTALLATION

12. Remove the two silver 75 OHM termination caps from the game package and screw them tightly onto the ANTENNA IN 75 OHM UNBAL port and the CH ¾ VHF OUT port located at the rear of the video disc player. See illustration.
13. Carefully pull the four black cables, located to the right of the video disc platform, out of the cabinet far enough to connect to the video disc player. Do not apply force when pulling on the cables.
14. Place the cable terminated with the F connector (the only connector with threads on the inside) onto the VIDEO OUT port and screw on tightly. NOTE: Be certain that the center pin goes into the center hole on the port. See illustration.
15. Plug the cable terminated with the black RCA plug tightly into the port labeled 1/L. See illustration.
16. Plug the cable terminated with the red RCA plug tightly into the port labeled 2/R. See illustration.
17. Plug the cable terminated with the ⅛" phono plug tightly into the port labeled EXT CONTROL. See illustration.
18. Route all cables to the right side of the video disc platform.
19. Lift the video disc player from the left and right sides and place on the video disc platform in the grooves cut out for the feet making certain that the cables do not get routed under the video disc player.
20. Lock the video disc player down with the metal lock-down bracket, placing the bracket from front to rear center of the player with wood screws. NOTE: Complete the B. CHECK- OUT procedure before continuing.
21. Close the back door and turn the game on. MAKE CERTAIN THAT NO CABLES ARE PINCHED IN THE DOOR
22. Be certain that the screen displays the disc initialization which includes four steps:
    (1) STOP DISC
    (2) START DISC

(3) SEEK FRAME
(4) High Score Table is displayed.

NOTE: The Disc initialization process can take as long as one minute.

B. CHECK-OUT

1. Carefully inspect the exterior of the game for any damage which might have occurred during shipment.
2. Unlock and open the rear cabinet door.
3. Check that all plug in connectors are seated firmly. The connectors are keyed so they will only go in one way.
4. Check that all cables are free of the back door.
5. Check for any loose wires.
6. Check for loose solder or foreign matter on switches and power supply assemblies.
7. Be certain all fuses are seated firmly.
8. Be sure transformer wiring corresponds to the supply voltage.
9. Refer to the GAME ADJUSTMENTS section of this manual to make all necessary game adjustments.

C. CONTROL PANEL REMOVAL (SIT-DOWN VERSION)

CAUTION: Before performing the Control Panel Removal, support the Control Pod from the player compartment to avoid the Pod from falling forward on its lower hinges.

1. Unplug the game.
2. Unlock and open the rear cabinet door.
3. From inside the rear of the cabinet, remove two ¼" nuts located on the wall behind the Control Pod.
4. Remove the Control Pod support and rotate the Pod down on its lower hinge.
5. Remove two ¼" nuts from the underside of the Control Pod.
6. Disconnect the Control Panel plugs A8J11/A8P11 and A9J2/A9P2.
7. Slide the Control Panel toward the player compartment.
8. For reassembly, reverse the above procedure.

CONTROL PANEL REMOVAL (UPRIGHT VERSION)

1. Unplug the game.
2. Unlock and open the coin chute door.
3. Reach in through the coin chute door and unlatch the four latches located at the top of the Control Panel.
4. Grasp the Control Panel at the front edge and pull it forward as far as it will go (approximately ¼").
5. Raise the front of the Control Panel approximately one inch above its supports and lift the entire assembly high enough to disconnect A9J2/A9P2.
6. Remove the entire Control Panel Assembly from the game.
7. The joystick and leaf-switches are now accessible for removal or cleaning.
8. For reassembly, reverse the above procedure.

D. MONITOR REMOVAL (SIT-DOWN VERSION)

1. Unplug the game.
2. Unlock the front glass with keyed lock located on the upper left outside of the cabinet in reference to sitting inside the player compartment.
3. Lift the front glass up and then out.
4. Remove the CRT frame.
5. Remove the filter glass by lifting up and then out.
6. Remove the four screws from the bottom lens lock.
7. Remove the lens lock board.

CAUTION: THE LENS SCRATCHES EASILY. PRACTICE EXTREME CARE WHEN HANDLING. AVOID TOUCHING THE RIDGED SURFACE OF THE LENS.

8. Pull the bottom of the lens forward to clear the frame and then pull out. When reinstalling the lens, be certain that the ridges are facing into the player compartment.
9. Remove the monitor mask.
10. Unlock and open the rear cabinet door.

11. Disconnect the video plug A17J1, the monitor power supply plug A12J3/A12P3 and the ground wires from the monitor chassis.
12. Remove the four bolts from the underneath side of the monitor shelf.
13. Remove the monitor from the front of the game, being careful to clear all cables from the CRT neck.
14. For reassembly, reverse the above procedure. NOTE: Reinstall the lens with the ridges facing the player compartment.

NOTE: The color monitor contains HIGH VOLTAGES delivering LETHAL quantities of energy. Do not attempt to service the monitor until you have shorted the anode plug on the picture tube to ground.

MONITOR REMOVAL (UPRIGHT VERSION)

1. Unplug the game.
2. Perform the control panel assembly removal procedure (Section C).
3. Unlock and open the rear cabinet door.
4. Disconnect the video plug A17J1, the monitor power supply plug A12J3/A12P3 and the ground wire from the monitor chassis.
5. From the Control Panel, remove the one nut and one washer from each of the four carriage bolts used to secure the monitor to the platform.
6. Remove the monitor from the rear of the game, being careful to clear all cables from the CRT neck.
7. For reassembly, reverse the above procedure.

E. SPEAKER ASSEMBLY AND MARQUEE REMOVAL (UPRIGHT ONLY)

1. Unplug the game.
2. Unlock and open the back door.
3. Unplug the A15-J1/P1 connector.
4. Unlatch the two latches on the rear of the Speaker Assembly Panel located inside the back door above the monitor.
5. On the front of the game, pull down on the lower molding under the marquee. The Speaker Assembly will lower to allow removal of the marquee.
6. Remove the marquee by lifting it upward out of its track. The Speaker Assembly and Illumination Assembly are now accessible for servicing.
7. Tilt the front of the Speaker Assembly downward while lifting the center upward. Pull the assembly straight out to remove. Be careful not to pinch the Speaker Assembly cable.
8. For reassembly, reverse the above procedure. When replacing the marquee:
   a. Tilt the front of the Speaker Assembly downward.
   b. Place the bottom of the marquee in the lower molding track on the front of the assembly.
   c. Apply slight pressure with your thumbs to the lower left and right corners of the marquee.
   d. Slowly raise the Speaker Assembly until the top of the marquee is in place in the upper track in the top molding.
   e. Be certain to reconnect the A15-J1/P1 connector and relatch the rear assembly latches.

F. AIR FILTER REMOVAL (SIT-DOWN VERSION)

CAUTION: CLEAN THE AIR FILTER MONTHLY. The air filter is used to filter out dust particles that could otherwise enter the inside cabinet and damage the game.

1. Unplug the game.
2. Unlock and open the rear cabinet door.
3. The filter and fan are located at the lower left corner by the rear door of the rear cabinet in reference to facing the inside of the rear cabinet. Slide the filter door to the right as far as it will slide.
4. Pull the top of the filter door out and pull the door up to remove.
5. Slide the filter out which is encased in a metal frame.

6. Clean the filter in a warm soapy solution.
7. For reassembly, reverse the above procedure. Replace the filter with the grill side facing up.

AIR FILTER REMOVAL (UPRIGHT VERSION)

1. Unplug the game.
2. Unlock and open the rear cabinet door.
3. The filter door is located at the center of the cabinet directly in front of the back door. Pull the filter door up to remove.
4. Pull the filter straight out.
5. Clean the filter in warm soapy water.
6. For reassembly, reverse the above procedure.

G. MONITOR LENS CLEANING (SIT-DOWN ONLY)

1. Unplug the game.
2. Unlock the front glass with keyed lock located on the upper left outside of the cabinet in reference to sitting inside the player compartment.
3. Lift the front glass up and then out
4. Remove the CRT frame.
5. Remove the filter glass by lifting up and then out.
6. Remove the four screws from the bottom lens lock.
7. Remove the lens lock board.

CAUTION: THE LENS SCRATCHES EASILY. PRACTICE EXTREME CARE WHEN HANDLING. AVOID TOUCHING THE RIDGED SURFACE OF THE LENS.

8. Pull the bottom of the lens forward to clear the frame and then pull out. When reinstalling the lens, be certain that the ridges are facing into the player compartment.
9. ON THE SMOOTH SURFACE ONLY: Clean with a very mild warm soapy water solution and a clean soft rag.

   ON THE RIDGED SURFACE ONLY: Clean with warm water only and a clean soft rag.
10. For reassembly, reverse the above procedure.

SECONDARY MONITOR INSTALLATION

If a second monitor is desired for extended viewing area in an arcade, the second monitor can be installed with the following changes:

1. On the A18 Color/Sync Board, change resistors R47, R48 and R49 from their current values of 180 OHMS each to 470 OHMS each.
2. Splice the wires going to the secondary monitor as close as possible to the A17J1 connector on the primary monitor.

If the characters or images on the secondary monitor are blurry or streaking, terminate the transmission wires at the A17J1 connector on the secondary monitor with 180 OHM resistors. To accomplish this, connect a 180 OHM resistor from Pin 1 (Red signal) on the A17J1 connector (on the secondary monitor) to pin 4 (Ground), a 180 OHM resistor from pin 2 (Green signal) to pin 4 and a 180 OHM resistor from pin 3 (Blue signal) to pin 4.

II. INITIALIZATION

TURN GAME ON

The Disc Spin Up starts. This process can take as long as one minute. The automatic procedure is as follows:

1. STOP DISC
2. START DISC
3. SEEK FRAME

The high score table will then be displayed.

The attract mode begins.

III. GAME OPERATION

A. GAME START

1. Insert coins into coin chute.
   a. Coin chute tune is played.
   b. Total credits are displayed on the screen.
2. Push the joystick to the left or right to begin either the fighter game or the bomber game respectively.
   a. Total credits are decreased by one.
   b. Game begins.

HOW TO PLAY M.A.C.H. 3

MILITARY AIR COMMAND HUNTER

CONTROL PANEL

The joystick controls the movement of the players plane. It can be moved in eight directions. The trigger on the joystick as well as the gun button on the Control Panel will fire a machine gun from the plane. The buttons on the joystick as well as the missile button on the Control Panel will fire missiles from the plane. Only four missiles can be in flight at one time. It takes five hits with the machine gun to destroy a target while it takes only one hit with the missiles. In the bomber game, bombs are dropped using the same button used for missiles.

STARTING THE GAME

After depositing the correct amount of coins for a credit, push the joystick to the left, until the cursor moves all the way to the left, to start the fighter game. Push the joystick to the right to start the bomber game. NOTE: If the joystick is not moved to the left or right, the fighter game will begin in 10 seconds.

FIGHTER GAME

Squeeze the trigger to stop the instructions from printing on the screen to start the game faster. Game play begins with the players fighter jet flying over enemy territory on a perilous mission to destroy the enemy. While flying in dangerous areas, enemy ground targets are sighted and must be destroyed. They can be shot with the players machine gun or hit with the players missiles. All ground targets are marked by a yellow dotted square around a marker depicting the type of enemy artillery the player is trying to destroy. All ground targets award 500 points.

Suddenly and without warning the enemy ground facilities begin to launch their own missiles at the players plane. They must be avoided or destroyed. Being hit by a missile loses one plane. Destroying an enemy missile awards 200 points.

Mountain sides are also a hazard. Avoid colliding with mountains during battle.

The enemy launches their own air attack on the players plane with helicopters and fighter jets. The helicopters fire missiles at the players plane. The missiles must be destroyed or avoided. Destroying a helicopter awards 1000 points. The fighter jets fly in front of the players plane and shoot a trail of flame from their jets which must be avoided at all costs. Destroying an enemy jet awards 500 points.

Later in the mission, the player may encounter some radioactive fields that produce deadly radioactive clouds. These clouds must be avoided.

BOMBER GAME

Squeeze the trigger to stop the instructions from printing on the screen to start the game faster. Game play begins with the players bomber plane flying over enemy territory on a new and different course than the fighter jet. While carrying out the bombing mission the player looks for enemy ground artillery to destroy. When they appear, the player drops bombs on the designated sights. Ground targets can only be destroyed with bombs. The maximum number of bombs in the air at one time is 8. All ground targets are marked by a yellow dotted square around a marker depicting the type of enemy artillery the player is trying to destroy. All ground targets award 500 points.

IV. GAME PLAY AND SCORING

In defense of their country, the enemy launches flak to destroy the players bomber. Flak explodes by itself in mid-air and can destroy the bomber by touching it. Flak cannot be destroyed and therefore must be completely avoided.

As a means of aeronautical defense, the enemy sends fighter jets to destroy the players bomber. A red marker on the top of the screen warns of approaching aircraft. The players bomber must not collide with these fighter jets and can destroy them with machine gun fire only. If an enemy fighter is allowed to fly behind the players plane, he will fire missiles at the players bomber. Destroying an enemy fighter awards 300 points. Destroying his missiles awards 1000 points.

A portion of the enemy territory has become radio active. Avoid the radioactive clouds.

ENDING THE GAME

The game ends when either all of the players planes are destroyed or the video disc has been completed. A successful mission is completed in approximately 15 minutes.

ATTACK STRATEGY FOR FIGHTER GAME

ENEMIES	COUNTER ATTACK	POINTS AWARDED IF DESTROYED	METHOD OF DESTRUCTION
Ground Targets	Shoot missiles at players plane	500	missiles machine gun
Helicopter	Shoot missiles at players plane	1000	missiles machine gun
Missiles	NOT APPLICABLE	200	missiles machine gun
Enemy Fighter Jets	Trail of flame	500	missiles machine gun
Radio Active Cloud	NOT APPLICABLE	NONE	NONE

ATTACK STRATEGY FOR BOMBER GAME

ENEMY	COUNTER ATTACK	POINTS AWARDED IF DESTROYED	METHOD OF DESTRUCTION
Ground Targets	Launch flak missiles	500	bombs
Flak	NOT APPLICABLE	NONE	NONE
Enemy Fighter Jets	Missiles if behind	300	machine gun
Missiles	NOT APPLICABLE	1000	machine gun
Radio Active Cloud	NOT APPLICABLE	NONE	NONE

V. SOUND

The Sound Board in this game has been programmed for sound and speech. This Sound Board cannot be replaced or exchanged with any other Sound Board.

VI. GAME ADJUSTMENTS/OPTIONS

A. CONTROL BOARD SWITCH ADJUSTMENTS

SWITCHES 1	2	3	LIVES	COST
OFF	OFF	OFF	3	FREE
ON	OFF	OFF	3	2
OFF	ON	OFF	3	3
ON	ON	OFF	3	4
OFF	OFF	ON	5	2
ON	OFF	ON	5	3
OFF	ON	ON	5	4
ON	ON	ON	5	5

SWITCHES 4	5	6	BONUS	1/NEXT/	DIFFICULTY
OFF	OFF	OFF	15K	20K	EASY
ON	OFF	OFF	30K	40K	EASY
OFF	ON	OFF	40K	50K	EASY
ON	ON	OFF	50K	60K	EASY
OFF	OFF	ON	30K	50K	HARD
ON	OFF	ON	50K	100K	HARD
OFF	ON	ON	80K	100K	HARD
ON	ON	ON	100K	150K	HARD

SWITCH 7 — ATTRACT MODE SOUND

OFF ..... NO SOUND
ON ..... SOUND

SWITCH 8 — DEMO MODE

OFF ..... NORMAL GAME PLAY
ON ..... INFINITE LIVES

B. SOUND ADJUSTMENTS

The audio output is controlled by the potentiometer mounted on the service panel assembly (located inside the coin mechanism door).

Turning the potentiometer counter-clockwise will decrease the volume. Turning it clockwise will increase the volume.

C. MONITOR ADJUSTMENTS

Normally, few if any adjustments are required for proper monitor operation. However, after any major repairs to the monitor chassis refer to the attached monitor manual.

WARNING: The Shield Top covering the Master Electronics Panel will have to be removed in order to make some adjustments to the printed circuit boards. This cover is used, in part, to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules. Failure to replace the Shield Top over the Master Electronics Panel when the game is in operation voids all warranties.

VII. BOOKKEEPING AND SELF TEST

SELF TEST

The self-test consists of five functions which may be used to identify problems in the video disc system and to change program parameters.

The self-test mode is entered by setting the self-test toggle switch located inside the coin door to TEST. A menu of available tests are displayed on the monitor. To return to the GAME mode at any time, set the toggle switch back to GAME.

The game will then re-initialize the video disc and return to its normal attract sequence.

Selection of tests is done with the push button switch labeled SELECT. Upon entering the test mode, a flashing arrow points to the first test selection. Momentarily depressing the SELECT button will advance the arrow through each selection one by one.

When the arrow is pointing to the desired test, the operator may begin that test by pressing the SELECT button and holding it down until the test appears on the screen.

Once a test has been selected, the operator can return to the main menu by holding down the SELECT switch until it re-appears. The five tests are as follows:

1. CONTROL PANEL

Colored squares are shown for each switch input, including each missile button, the slam switch and the trigger on the joystick. An open switch is shown as blue, while a closed switch is shown as yellow. The joystick switches are displayed as four blue squares in the bottom right corner of the screen forming a diamond. Movement of the joystick will cause the appropriate square to change color. Pushing the joystick at an angle will cause the two appropriate squares to change color to yellow. The slam switch indicator should normally be yellow, if not, the game will not run.

For each coin mechanism, a digit is displayed (initially 0). Inserting a coin into a coin chute will increment the appropriate value without affecting the coin meter.

2. DIP SWITCH SETTINGS

A functional description of the eight position Dip Switch located on the Logic Board Assy, underneath the far right side of the Interface Board is displayed. Changing the switch settings will cause an immediate update of the description displayed on the screen. All of the possible switch combinations are shown. Any switch that is "ON" is displayed by "ON" and any switch that is off is displayed by a dashed line (-). The arrows indicate the current switch settings. Switches 1, 2 and 3 adjust lives per game, number of coins required to start the game and number of coins needed represented by each coin switch closure.

Switches 4, 5 and 6 adjust the first bonus life, the next bonus life and the difficulty level.

Switch 7 adjusts the desired attract mode sound setting.

Switch 8 sets the Demo mode (infinite lives).

See VI. GAME ADJUSTMENT/OPTIONS A. CONTROL BOARD SWITCH ADJUSTMENTS.

3. BOOKKEEPING

Selecting this test will display a menu of five functions. Pushing the SELECT button momentarily will move the arrow on the screen to the desired function. When the arrow points to the desired function, hold the SELECT button down until that function is displayed.

DISPLAY SCORE COUNTS — Two separate tables (one for the fighter game, another for the bomber game) are shown one at a time. Each table has 18 categories of score values by thousands (K) and a count associated with each category. The fighter high score table is shown first. To move to the bomber high score table, press the SELECT button momentarily. The count represents the number of plays in which the score at the end of the game fell into that category. In addition, a high score, low score and average score are shown along with the total number of plays on which the average is based. To clear the table, press the MISSILE FIRE button on the control panel and return to the menu by holding down SELECT.

DISPLAY TIME COUNT — Same as above except each category represents play times in seconds. The high, low and average are given in minutes and seconds.

DISPLAY ROUND COUNTS — This category displays the Fighter (or Bomber) Disc Achieved. Each category represents what percentage of the disc was played per game. The number next to the percentage represents the total number of games ending within that percentage range.

RESET HIGH SCORES — Selecting this test will reset the high score table.

4. HARDWARE TESTS

Selecting this test will display a menu of five functions. Pushing the SELECT button momentarily will move an arrow on the screen. When the arrow points to the desired function, press the SELECT button and hold it down until the test appears.

MONITOR ADJUSTMENT — Four patterns can be displayed on the screen for adjusting monitor color, brightness, contrast and convergence. The patterns are: color bars, a cross-hatch, a gray scale and a dot pattern. By momentarily pressing the SELECT button, the four patterns may be cycled through.

MEMORY TEST — For each RAM memory chip: an OK or an NG (no good) appears signaling that the chip is good or bad respectively.

Check sums are displayed for each ROM memory chip. If you have a suspect ROM, refer to your distributor for the correct check sum number.

SOUND TEST — After selecting this test a count will appear on the screen representing the various sounds that are produced by the game. There will be 29 different sounds produced and the screen count will repeat to 01. Pressing either Control Panel button will suppress all sound output and speed up the count so a particular sound can be investigated.

Note: The count on the screen represents the binary signal code that will be sent to the A6 Sound Board through the sound input lines on the A6J4 connector. When executing the Sound Test sequence, there will be no sounds produced on counts 10, 12, 13, 14, 16, 17, 13, 25-32, 38, 44, 46, 47 and 48-56. These numbers are either not used or affect other sounds. These number assignments are subject to change.

EXTENDED FOREGROUND TEST — Selecting this test will display all of the foreground characters on the screen. A limited number of characters are shown on each screen. Pressing the SELECT button momentarily will display the next screen of characters.

5. VIDEO TESTS

Selecting this test will display a menu of four functions. Pushing the SELECT button momentarily will move the arrow on the screen. The selected test will automatically begin when the arrow is pointing to it.

NOTE: If the game has been powered up in the test mode, the SPIN DISC UP function under DISC CONTROL may need to be performed. See DISC CONTROL below.

GEN LOCK TEST — Selecting the GEN LOCK TEST will display a menu of three functions.

(1) GRAPHICS ONLY — This test shows the computer display only. There is a black background with the computer generated color bars and foreground objects showing only. The foreground objects are within the color bars.

(2) DISC AND GRAPHICS — This test shows the computer display foreground and the disc display background. The computer generated foreground objects are seen against the video disc background. Be sure the foreground objects are clear and that all computer generated color bars are close in hue to the disc generated color bars. To adjust the disc generated background color bars, adjust the following on the Color/Sync Board: R37 (tint adjust), R38 (color saturation adjust), R27 (brightness adjust) or R35 (contrast adjust).

(3) NO VIDEO — This test shows a dark screen displaying no video.

COMMAND CONTROL — Selecting this test will display a menu of two functions.

VII. BOOKKEEPING AND SELF TEST

Pushing the SELECT button momentarily will move an arrow on the screen. When the arrow points to the desired function, press the SELECT button and hold it down until the test appears.

(1) REPEATED STEP FORWARD — After selecting this test, pushing the SELECT button momentarily will step the disc frame forward one frame repeatedly and also triggers the Sound Board to produce a 2.5 KHz pulsing tone when R22 (clock burst adjust) on the Interface Board is adjusted properly. If the disc does not step forward check the cables connecting to the Interface Board for correct placement and a tight fit and check the EXT CONTROL cable connected to the rear side of the video disc player. If the disc still does not step forward, adjust R22 on the Interface Board until the 2.5 KHz pulsing tone is heard.

(2) SPIN DISC UP — Selecting this test initializes the disc. This prepares the disc for video tests if the game was powered up in the test mode. The initialization automatic sequence is as follows: (a) the disc is brought to a halt, (b) the disc is spun and brought up to operating speed, (c) the system seeks out frame #1.

FRAME DECODER — Selecting this test will display a menu of two functions. Pushing the SELECT button momentarily will move an arrow on the screen. When the arrow points to the desired function, press the SELECT button and hold it down until the test appears.

(1) STILL FRAME DECODER — After selecting this test, the video disc player seeks frame #12345. The number in the upper left corner of the screen is the actual current disc frame number. Directly below it is the current frame number the computer recognizes. The two numbers should match. When they do, the Sound Board is triggered. This allows adjustment of R204 (frame number level) on the Color/Sync Board. Adjust R204 until a constant uninterrupted tone is heard. This constant tone will indicate that R204 is adjusted correctly.

(2) PLAY FRAME DECODER — This test is the same as the STILL FRAME DECODER test except the disc is playing. Adjust R204 on the Color/Sync Board until a constant uninterrupted tone is heard again.

AUDIO TRACK DECODER — Selecting this test will display a menu of two functions. Pushing the SELECT button momentarily will move an arrow on the screen. When the arrow points to the desired function, press the SELECT button and hold it down until the test appears.

(1) AUDIO CHECK SUM TEST — Selecting this test will display the results of a 30 second test of the Audio Track Decoder. If "AUDIO TRACK TEST FAILURE" appears on the screen, it is suggested to proceed to and complete the AUDIO TRACK DECODER ADJUSTMENT test and then rerun the AUDIO CHECK SUM TEST to insure Audio Track Decoder integrity.

(2) AUDIO TRACK DECODER ADJUSTMENT — Selecting this test will first ask you to move a jumper on the Interface Board from JP3 to JP2 and to turn up the volume control. Press the SELECT button momentarily to start the test. A tone will sound to signify the start of the adjustment period which continues for approximately 15 seconds. After the 15 second period, the tone will stop to indicate that the computer is re-searching the disc for the beginning of this test to repeat it automatically. When the test automatically restarts, the tones begin again and adjustment can continue if not completed. This test will continue to recycle until the SELECT button is pressed and held down. If R6 on the Interface Board is not correctly adjusted, two tones will be heard instead of one. Adjust R6 until only one tone is heard. When this is accomplished, press and hold the SELECT button down.

The tone is now heard again so that R39 on the Interface Board can be adjusted. Follow the same procedure to produce one tone only if two are heard. When completed, press and hold the SELECT button down. Rerun the AUDIO CHECK SUM TEST.

WARNING: BE CERTAIN TO REMOVE THE JUMPER FROM JP2 AND REPLACE ON JP3, LOCATED ON THE INTERFACE BOARD ASSY

VIII. GENERAL INFORMATION

A. PRINTED CIRCUIT BOARDS ARE DESIGNATED AS FOLLOWS:

A1 Logic Board Assy.

A2 Interface Board Assy.

A3 Power Supply Assy.

A6 Sound Board Assy.

A8 Filter Board (I and II)

A18 Color/Sync Board Assy.

B. WIRE COLORS ARE SHOWN AS NUMBERS:

0 Black	5 Green
1 Brown	6 Blue
2 Red	7 Purple
3 Orange	8 Gray
4 Yellow	9 White

For example, 688 is a BLUE- SLATE-SLATE striped wire.

C. FUSES

BOTTOM PANEL

F1	115V AC 60 Hz (Primary Power)	4 Amp
F2	6.3V AC (Coin Chute Lamps)	1 Amp
F3	Monitor	2 Amp SLO-BLO
F4	9V AC (+5V DC)	12 Amp SLO-BLO
F5	15V AC (+12V DC, -12V DC)	2 Amp SLO-BLO
F6	15V AC (+20V DC)	2 Amp SLO-BLO
F7	Audio Amplifier Supply	1.5 Amp SLO-BLO
F8	Fan	3/16 Amp SLO-BLO

CABINET FUSE

F9	Video Disc	2.5 Amp SLO-BLO
F10	Rear Fan	3/16 Amp SLO-BLO

IX. THEORY OF OPERATION

SYSTEM OVERVIEW

Mylstar Electronics, Inc. Video Disc Graphics System is a character based system controlled by the Intel 8088 16-bit microprocessor for state of the art design. The graphics state machine is driven by a 10 MHz clock derived by dividing down a 20 MHz crystal or from the VCO (Voltage Controlled Oscillator) on the Color/Sync Board. The foreground generator can drive 63 individual, independent objects whose size is 16 pixels by 16 lines, selectable from 256 foreground objects, at any frame time. All of these objects have their own level of priority, which means that there are 63 planes of depth. A double line buffer is used to drive the video information.

The background generator is character oriented. The characters are determined by an 8 pixel by 8 line matrix, which can be selected from a 128 character set (when RAM is used for the character generator) or from a 256 character set (when ROM is used instead). Both background and foreground objects can be displayed with 16 different colors selected from a total of 4096 possible colors during any given frame time. The dot resolution of the system is 256 pixels by 240 lines.

All horizon and target information is encoded for each video frame and stored on audio channel 2 of the video disc. During game play, the video frame decoder reads the frame number from the video on the video disc so that the computer system knows exactly what frame is being displayed. Knowing the frame number, the computer system accesses the target data buffer describing object position and/or nature of that particular frame target.

Mylstar Electronics, Inc. utilizes a Pioneer LaserDisc™ brand video disc player and reflective disc. The video disc has encoded composite video information including picture, synchronized pulse and audio data. The pulse data identifies a unique frame number pre-assigned to each video frame.

The video disc player also produces two completely discreet audio channels from the audio data on the reflective disc. Audio is stored on channel 1/L while target data is stored on the channel 2/R.

The audio channel one is routed to an audio summer on the Sound Board while the audio channel two is routed to the audio decoder on the Interface Board.

The composite video signal is sent to the sync separator (U10) and to the color decoder (U1) on the Color/Sync Board. The color decoder decodes the chrominance and luminance from the composite video signal and produces an RGB signal.

The RGB output from the computer system and the RGB signal from the video disc are multiplexed (U2) and sent to the monitor.

The composite video signal from the video disc is asynchronous with the rest of the system, especially the video produced by the computer system. The composite sync is separated from composite video by the sync separator to produce the horizontal and vertical synchronization signals. The sync separator produces an external vertical sync pulse, EXT VSYNC, which resets the vertical counters causing vertical synchronization between the computer graphics image and the video disc image. The sync separator also produces an external horizontal sync signal, EXT HSYNC, which is coupled to a phase comparator (U6) of a phase locked loop (PLL) circuit also on the Color/Sync Board. The PLL also includes a voltage controlled oscillator (VCO) (U5).

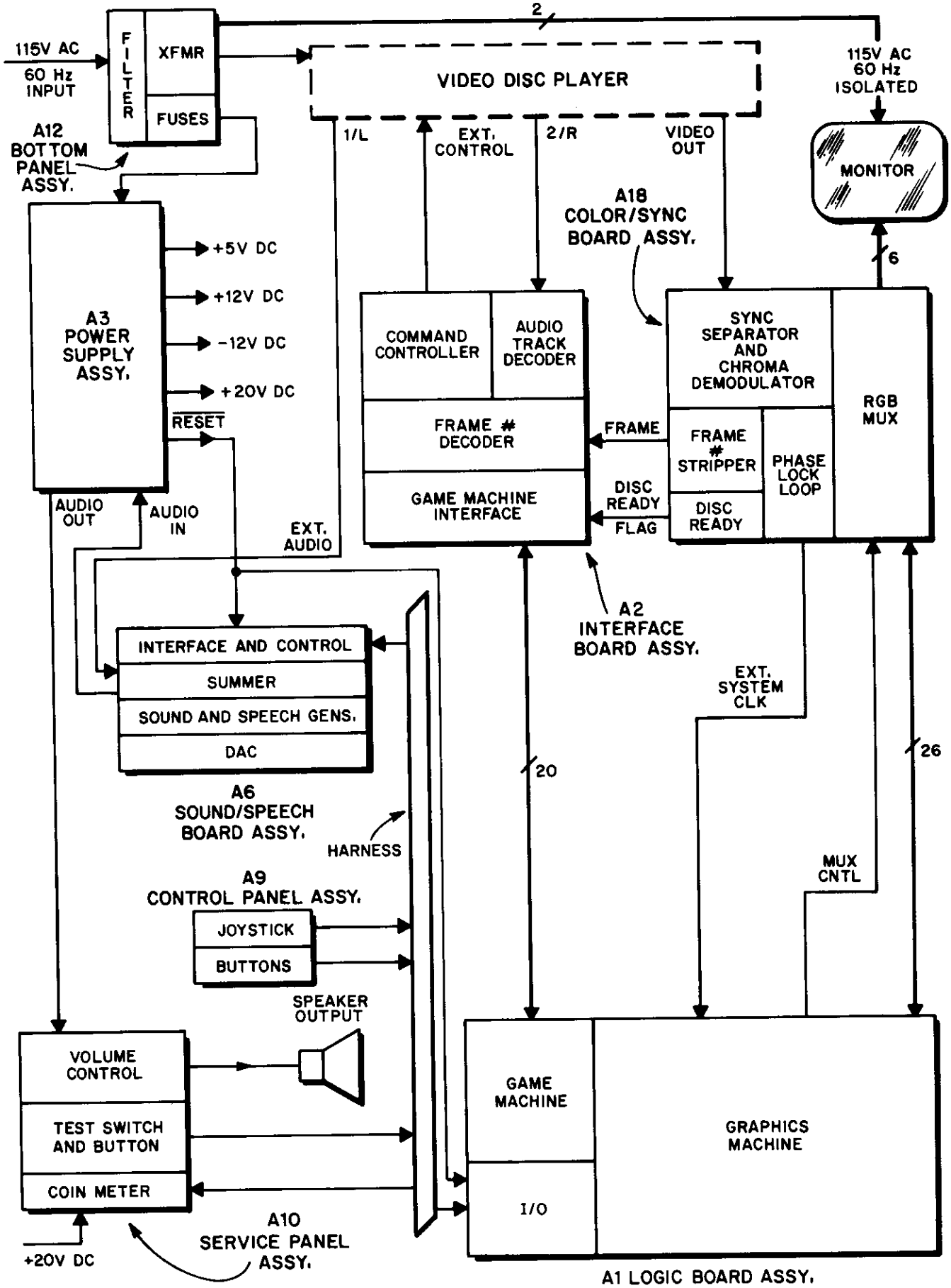
Besides the EXT HSYNC, the phase comparator also receives a horizontal synchronous signal which is related to the system clock of the computer graphics system. The comparator compares both signals for phase and frequency differences and produces a difference signal. The difference signal is filtered by the loop amplifier and sent to the VCO. The VCO then generates a signal, EXT CLK, which becomes the system clock of the computer graphics system.

BOTTOM PANEL ASSEMBLY

The input AC line voltage is filtered and wired to the 115V AC primary winding tap and the common tap of the transformer on the Bottom Panel. The secondary winding supplies five separate voltages. The isolated 115V AC supplies the monitor voltage as well as the Illumination Assembly voltage (where applicable).

The 9V AC RMS winding is full wave rectified and filtered to +11.5V DC average voltage. It is directly routed to the Power Supply via the Filter Board. The 6.3V AC RMS fused winding is sent to the front door to operate the coin chute lights. The

IX. THEORY OF OPERATION



SYSTEM BLOCK DIAGRAM

15V AC as well as the 9V AC windings are both routed directly to the Power Supply via the Filter Board.

POWER SUPPLY ASSEMBLY

The Power Supply, used to supply all voltages, is extremely tolerable to input line voltage variations. All output source voltages are guaranteed to be stable for line voltages varying from 95V AC to 135V AC 60Hz. The regulated logic +5V DC level is rated at 6 amps maximum and includes over-voltage crowbar protection. Four LED's on the Power Supply Board indicate that the associated voltages at the outputs are present.

The +11.5V DC entering the Power Supply Board is regulated to +5V DC by Q11, Q12 and U11 and is adjustable by VR1. R15 and VR1 along with R16 divide the regulator output voltage to +2.5V DC at the reference pin of U11, the programmable zener. As the output voltage rises, the voltage on the reference pin on U11 will rise. To compensate for the rising,output, U11 draws more current away from the base of Q12. This in turn turns off Q11 which drops the output voltage. As the output voltage of the regulator falls, the reference pin voltage falls, turning off U11. This will increase current flow through Q12 which in turn will increase current from the emitter to collector of Q11, raising the output voltage.

The over-voltage crowbar circuit mentioned earlier consists of C14, D12, R17, R18 and the SCR. The SCR requires 1.4V gate to cathode in order to turn on. The zener is rated at 5.6V. Therefore a voltage of 7V on the +5V DC line will trigger the SCR (7V-5.6 rated zener volts =1.4V). Once the SCR is on, the +5V DC line is shorted to ground, causing the fuse to open, preventing over-voltage damage to the TTL. R17 is a current limiting resistor for the SCR and R18 is the zener resistor. C14 filters out spikes that could trigger the SCR.

The 9V AC RMS is rectified and filtered and supplies the Audio Amplifier, LM2002, with unregulated +12V DC. The input Audio comes in on pin 3 of P7 and is 5V AC peak to peak (to keep a good signal to noise ratio). This signal is attenuated by R51 and R52 by fifty times and is fed to C52, the amplifiers input.

The 220 ohm R54 and 2.2 ohm R55 set the closed loop gain of the LM2002 by the equation A_V=1+R220/R2.2=101. Therefore the overall system gain is 101/52=1.94. R53, C55, R56 and C57 are compensation networks at 1 MHz and 10 MHz to keep the LM2002 unconditionally stable. C54 is the low frequency feed back capacitor. C58 is the output capacitor blocking the DC bias of the amplifier so that the output voltage on the speaker can swing above and below ground. The output apears at pin 3 of P6.

The center-tapped 15V AC RMS is utilized to supply three voltages. It is full wave rectified by D41 and D42 in order to supply the +20V DC average voltage used for the coin meters. It is also full wave rectified by D31 through D34 in order to supply the plus and minus 12V DC. The positive side of the bridge feeds the LM340K (U31) +12V DC regulator at 1 amp, while the negative side of the bridge is sent to the LM320 (U41) which regulates the -12V DC at 0.1 amp. D36 and D44 are used as protection diodes in the event that the output or the regulator exceeds the input.

POWER SUPPLY RESET CIRCUIT

The Reset Circuit provides graceful power-up and power-down for the processors on the main Logic Board and Sound Board. It does this on power-up by holding the processors in reset until the +5V DC has settled and on power-down halts the processors before the +5V DC has begun to collapse. D71 through D74 full wave rectify the AC voltage that feeds the +5V DC regulator. This full wave voltage continually retriggers U71 at pin 4, the CMOS monostable, until the line voltage is removed. On power-up the full wave voltage charges C75 through R74. Until the voltage on C75 reaches the CMOS logic high threshold, the monostable U71 is held reset. This holds the processor reset to allow time for the +5V DC logic supply to settle.

Q71 and Q72 amplify and translate the CMOS level to drive multiple TTL loads.

D75 and C72 make up the power supply for the monostable from the full wave voltage.

R72 and C73 make up the timing components for U71 and are set for approximately 11 ms.

LOGIC BOARD ASSEMBLY

A 5 MHz dot clock drives a 9-bit Horizontal dot Counter (S16, S17 and T17) and an 8-bit Vertical Line Counter (G17 and K16). The horizontal counter

counts from 0 to 255 during active scan lines and 256 to 317 during the horizontal blanking time. When the horizontal counter reaches 317, it resets to zero. At the beginning of the horizontal blanking time (horizontal counter=256), it increments the vertical counter. The vertical counter counts from 0 to 239 during active vertical blanking time.

The watchdog timer (A3) will reset the microprocessor unless it receives a pulse through the output port (B9) at least every 256 msec. The BLANK signal is generated from T14 pins 2 and 3. Pin 2 is the VBLANK input and pin 3 is the HBLANK inputs. VBLANK is produced when G17 reaches its maximum count or when the video disc VSYNC presets the outputs of G17 high. H17 then generates a low because all of the G17 outputs are high. Multiplexer V15 selects which VBLANK signal is inverted by T15 and sent to pin 2 of T14. The HBLANK is generated by pin 14 of T17 which is the most significant bit of the horizontal counter. The BLANK signal is inverted by K17 which turns on Q81 providing +5V DC to the emitters of Q82 through Q87, the color output transistors.

The 20 MHz crystal divided by two is the crystal system clock signal generated at pin 5 of V14. Multiplexer V15 selects between the crystal system clock and the video disc VCO clock. This signal becomes the CLK signal which clocks all of the logic timing and produces the HCLK signal from pin 9 of V14 which clocks the horizontal counters and latches.

Foreground generation on the System is initiated with three foreground registers (H1, H2 and H4) all addressed via the microprocessor through program control. These registers are the Foreground Horizontal Position Register (H1), the Foreground Object Select Register (H2) and the Foreground Vertical Position Register (H4).

When the appearance of an object is required on a scan line, as detected by the Vertical Position Detector, the address generated by the Foreground Horizontal Position Register is copied into the Line Object Position RAM (N1-N4) and the address generated by the Foreground Object Select Register is copied into the Line Object Select RAM (S1-S6). The Line Object Position RAM contains the horizontal position of the object for the next scan line while the Line Object Select RAM contains the address for the Object ROM to address the desired object.

Since the foreground object size is 16 pixels by 16 lines, the Vertical Position Detector must generate enable pulses for 16 successive lines. The high order 4 bits of the Foreground Vertical Position Register and the Vertical Counter are summed (H5) and feed the Line RAM Enable Pulse Generator (H6 and S8). When the sum values of H5 are all high, the write enable is generated. This pulse enables the transfer of data from the Foreground Horizontal Position Register to the Line Object Position RAM as well as the transfer of data from the Foreground Object Select Register to the Line Object Select RAM via the read/write (WR) signal (FBA4) and the chip select (CS) signal (S2) from the multiplexer (M9). For each pulse generated, information for the next scan line is loaded into the Line RAM.

When the Line RAM Enable Pulse Generator generates a pulse, it increments the 5-bit Line RAM Address Counter. This counter produces the addresses for the Line Object Positon RAM's. When the Line Object Position RAM is being read, the 8-bit Line Buffer Address Counter (N5 and N6) is loaded (every 1.6 usec). Before any new horizontal information can be loaded into the Line RAM, the counter must increment 16 times in order to address the 16 pixels that the foreground object will occupy that frame time.

The low order 4-bits of the Foreground Vertical Positon Register and the Vertical Counter are summed (K5) and address the object information to the Foreground Object ROM (T4, T5, T6 and T8) via the multiplexer (M5) and the Object ROM Address Latches (T1-T3). The Foreground Object ROM's receive their addressing from three sources: (1) the high order 8-bits from the Foreground Object Select Register, (2) 4-bits from the Vertical Position Detector and (3) the least significant bit (RA0) comes from the 800ns counter (V12). This counter will output every 4 clock cycles. The information out of the Object ROM's is loaded into four parallel to serial shift registers (V4, V5, V6 and V7). Every clock cycle the outputs of the four shift registers are checked for data. If any output data, a write enable pulse (T12, T13 and T9) is generated allowing data to transfer to the Line Object Buffers.

The Background Character Registers (H7) data is

copied into the Background Buffer RAM (H10) during the first half of the vertical blanking time through DMA transfer (H9). Once the data is read by the Buffer RAM, the Character Register is ready to be loaded with new information. The data in the Buffer RAM is an 8-bit object number. This object number addresses the Background Character ROM (H12 and H13) which contains pixel definition for the background character. The Character ROM will output 8-bits of information for two pixels for the 8 pixel by 8 line character. The horizontal counter, H1 and H2, and the vertical counter, V0, V1 and V2, are used so that the background object is displayed at the correct vertical and horizontal positons on the screen for each frame.

The dual line buffers are 256 x 4-bit RAM which contain one scan line of foreground object information. While one line buffer is loaded for the next scan line, the other is being read. These 4 bits of information form the foreground video output.

Pin 2 of A8 (F/B priority signal) is used to choose the dominance between foreground and background objects in the video arbitrator which consists of N11 and S12. A high on multiplexer N12, pin 10, will give background priority while a low gives foreground priority. The inputs to both 5-input NOR gates of N11 are the 4-bit color numbers needed to color one pixel. All colors have priority over color zero. If either of these pixel color numbers are zero, then a logic high is produced at the output of the NOR gate. N11, pins 5 and 6, are fed to the inputs of N14 (NAND gate) and then latch at dot time by V9 (D flip flop). Only when both the background and the foreground colors are zero, will the output of V9 be a logic low. This signal is sent to V15 (multiplexer) and becomes MUX CNTL. When MUX CNTL is a logic low, the video disc's RGB is selected. When MUX CNTL is a logic high, the computer graphic RGB is selected.

The code to be used for the pixel is transferred to the color registers M13, M14 and M15. The color register package is 16 x 12-bits (4-bits for red, 4 for blue and 4 for green). The registers are loaded with the 4-bit color code during the vertical blanking time only. The selected 4-bits by the foreground/background arbitrator is the address for the color RAM. In other words, it is not the data for the picture, but the location of the desired color. The color registers output is sent to the monitor through the D to A converter which consists of R93 through R104 and Q82 through Q87.

COLOR SYNC BOARD

The Color/Sync Board has 6 major functions:

1) Sync separation of HSYNC and VSYNC from the video disc.
2) Strip the frame number from composite video and convert it to a TTL compatable signal.
3) Composite video to RGB from the video disc.
4) Multiplexing of video disc RGB and Graphics RGB.
5) Phase Lock Loop to adjust Graphics System Clock so that the video discs HSYNC and Graphics HSYNC match in phase and frequency.
6) Generation of video disc Ready Flag and VDVSYNC.

SYNC SEPARATOR

1V_{pp} composite video from the video disc player comes into J5 via a 75 ohm coax cable through C1 to an inverting amplifier (Q1 and Q2) with a gain of 5. This 5V_{pp} composite video is DC restored with C4, R9 and CR102. The DC restored video is sent to a dual high speed comparator(U10) so that composite sync and the frame number are stripped from composite video. The composite sync is sent to U7 to remove the vertical serrations for the PLL, also to an inverter and then an LRC network consisting of R12, L1, C7 and C10 which delays the HSYNC so as to line up with the Chroma burst signal needed by the Chroma Demodulator (U1). Composite sync is also sent to R100, C17, R15 and C8, which is the integrator to separate VSYNC. Q4 and Q104 are the vertical sync amplifiers.

STRIP THE FRAME NUMBER

The video frame number decoder includes a frame number stripper (U10) that receives the composite video signal. Potentiometer R202 adjusts the comparator voltage level. The stripper also receives the horizontal and vertical sync information contained on the disc, the EXT HSYNC signal and the EXT VSYNC signal. The EXT VSYNC resets the D flip flop (U9), therefore enabling the output of the high speed comparator (U10) at the next HSYNC pulse. When the output of the comparator goes high, the D flip flop (U9) will set and

therefore disables the comparator output at the next HSYNC pulse. Because the 24-bit Phillips frame number code is only present during the odd field of vertical blanking, every other series of pulses will be the 24-bit code. The output from the stripper is fed to J7 and then to the Interface Board which detects the frame number and stores it in latches for game machine use. By using the test mode in the game, the frame number decoder can be adjusted via potentiometer R202.

COMPOSITE VIDEO TO RGB FROM THE VIDEO DISC

Before explaining this portion of the board, several words should be defined:

Chrominance — The colormetric difference (dominant wavelength and purity) between any color and a reference "white" of equal luminance. In other words, the color information in the television picture.

Luminance — Luminous intensity reflected or emitted by a surface in a given direction per unit of apparent area. In other words, the black and white portion of the television picture.

Composite video from J5 passes through C101 to the inverting amplifier with a gain of 3 consisting of Q101 and Q102 and associated components. This signal is sent through R19 to a 3.58 MHz trap consisting of L2 and C110 to remove the chrominance signal from composite video leaving only the luminance signal to pass through L4, DL1, L3 and C26 to U1, the Chroma Luma-Processor.

The inverted composite video from Q102 is also sent through R21 and C22 to T1, a 3.58 MHz bandpass transformer. This removes all luminance information from composite video leaving only the Chrominance to pass through C24 to U1, the Chroma-Luma Processor. The chrominance signal passing through the bandpass transformer is delayed in time. This delay is compensated by the Delay Line, DL1, so that the luminance signal arrives at U1 at the same time the chrominance signal does.

The Chroma-Luma Processor decodes the composite video to RGB appearing at pins 26, 27 and 28 respectively. These signals are restored and sent to the Analog multiplexer (U2) to be multiplexed with the RGB from the graphics system.

ANALOG MULTIPLEXER

The Analog Multiplexer multiplexes the RGB from the graphics system and the RGB from the decoding of video disc composite video. The Analog Multiplexer is controlled by the signal MUX CTRL from the Graphics Board via J2. This signal is delayed slightly to compensate for the access time of the color RAM and the D to A conversion on the Logic Board.

PHASE LOCK LOOP

Phase Lock Loop (PLL) circuitry is generally made up of a phase comparator, loop filter and a VCO (Voltage Controlled Oscillator). The phase comparator (U6) compares the phase and frequency of two digital signals and produces an error signal at pins 5 and 10. The loop filter composed of Q202, R43, R43A, C40, C21, R45 and R44 filter the digital error signal to a DC value the VCO can use. The VCO (U5) takes a DC voltage at pin 2 and produces a TTL compatable frequency at J1. This frequency is the system clock for the graphics state machine. The graphics state machine clock is divided down via TTL counters to produce HSYNC which is sent to one of the inputs of the phase comparator (U6) This closes the loop for the PLL. The reference frequency to the phase comparator is DHSYNC, which is the horizontal synchronization signal stripped from the video disc composite video.

The action of the PLL is to adjust the graphics system clock frequency at J1 to eliminate the phase and frequency difference between the graphics system HSYNC and the video discs DHSYNC. This is what makes the overlay of the computer generated graphics over the video disc background possible.

If the HSYNC signal received by the phase comparator from the computer system is slower than that received from the sync separator from the video disc, the difference signal fed to the VCO forces the VCO to speed up, and vice versa. This produces signals from the video disc and the computer system that are synchronous so that the two can be multiplexed for display on the monitor.

GENERATION OF THE DISC READY FLAG

The Disc Ready Flag tells the program logic that valid composite video is being produced from the video disc player. This signal is produced by using DVSYNC (the vertical sync pulse stripped from

composite video) to trigger a retriggerable monostable(U4).If DVSYNC is present with a 16 msec period, the Disc Ready Flag will be high.

PULSE SHAPING OF DVSYNC FOR THE VDVSYNC SIGNAL

The video disc produced image is larger vertically than the computer graphics image. The monostable (U7)produces a pulse width from DVSYNC which places the graphics image vertically in the middle of the video disc image. If no pulse is on the output of pin 12 of U7 when Gen Lock is called for, the picture will roll vertically.

INTERFACE BOARD

The Interface Board is the game machines interface to the video disc player. The board's four functions are:

1) Frame number decoder
2) Audio track decoder
3) Command controller
4) Disc ready flag

FRAME NUMBER DECODER

The 24-bit Phillips Frame Number Code is stripped from the video and is received at TTL levels from the Color/Sync Board on J7. The frame number code is squared up and inverted by A2 (Schmitt inverter). This signal is sent to a network of C29, R30 and A2 (positive edge detector), an inverter and another positive edge detector. These voltage spikes are summed by A4 (NAND gate) so that U5 can strip the clock of the frame data. The positive and negative edge voltage spikes are also inverted by A3 and summed with the clock to set up Set and Reset pulses for the D flip flop (B3). The D flip flop strips the data from the frame number signal for the shift registers B1, G1 and H1. The four input NAND gate detects a valid frame number and produces the clocking signal that latches the frame number into the latches B2,G2 and H2. The frame number is then read into the game machine via the data bus and strobes IP5, IP6 and IP7.

AUDIO TRACK DECODER

The audio track decoder on the Interface Board, receives the data from the audio channel 2. It decodes the signal to extract digital data, and stores data in RAM until the computer system is ready to read it. The audio track decoder includes an edge comparator (X4) that receives data from the audio channel 2. The comparator is a zero-crossing detector which produces a pulse for all transistions through ground.

One output of the edge comparator is coupled to a data detector (S2). The detector determines whether an edge is detected between clock pulses from the output of the edge comparator. A detected edge indicates that a "1" was received by the edge comparator. When that occurs, the data detector generates a high to be clocked into a serial to parallel (K1) converter via the clock from the clock detector.

Audio track 2/R of the video disc player is a 1 volt peak to peak signal which comes into J3 through C2 to a biasing network composed of R10 and R11 to a low pass filter made up of R36 and C10 to the zero crossing detector (X4). The pulse train at the AND gate, pin 8 of S4, is high when the input wave passes through ground. This signal is sent to E3, M5 and V5 so that the clock and break in transmission signals can be formed. The data is stripped off by A4 and S2 and sent to the serial to parallel converter, K1.

The parallel data is sent to the bus transceiver (M1, N3 ane N2) which detects the buffer sync byte, 67 (hex). A high pulse is produced at N2, pin 2, when the buffer sync byte is detected. This high is inverted by the NAND gate (S3) and clears the ready flag D flip flop (V4) and the RAM address counters (V3, V2 and V1) through the AND gate (S4). The RAM address counters sequentially address the RAM (S1) to store the data from the audio track for the game machine's later use. The clock for these counters came from two places, the data clock divided by 8 via N4 and the game machines address strobe shaped through B4. These clocks are multiplexed through the three NAND gates (S3) and controlled by the ready flag signal. The game machine reads the data through the Bus transceiver (K2) and strobe STB2.

COMMAND CONTROLLER

The Command Controller is the means by which the game machine sends instructions to the video disc player i.e., play, reject, still/step, etc. The 555 timer produces a 38 KHz clock signal when pin 4 is high. The clock can be calibrated by moving JP14 from normal to test and adjusting R22 until the period of the signal at pin 3 is at 26us. This is the clock to the counter chain made up of X2, W1 and X1.

X2 is the burst counter which strobes W2 to gate 10 clock cycles to the output. W1 is the data to period counter. If the data from M2 pin 9 is a logical high, the W1 is preset with an 8 which is approximately 2.1 ms. If the data is a logical low, W1 is preset with a 4 which is approximately a 1.05 ms period. X1 is the bit counter which counts 11-bits and sets the end of transmission flip flop (W2).

M2 is an 8-bit shift register that serializes the command byte from the game machine to the video disc player. Q1 and Q2 are output amplifiers.

DISC READY FLAG

The Color/Sync Board sends a TTL level signal to E2 on the Interface Board called the Disc Ready Flag. This signal is high when the disc player is producing valid video.

SOUND BOARD

The MA-495 Sound Board consists of two 6502 microprocessor systems, a dual DAC, an L.P.C. speech generator, two programmable sound generators, input ports to receive commands from the game Logic Board, external audio input and a low level audio output, which is sent to the MA-479 Power Supply Board for amplification.

The Sound Board requires three supply voltages: +5V DC, +12V DC and -12V DC. In addition a power up reset signal is required from the Power Supply Board.

SYSTEM CLOCK

A 4 MHz oscillator is configured with R11, R12, C14, C15, C22, XTAL-1 and T1. R21 and C22 are optional. This 4 MHz clock is divided by 4 to a 1 MHz clock for both processors' clock input, pin 37 of N1 and T3. A 2 MHz clock from S1 pin 14 is sent to the two AY-3-8913 Programmable Sound Generator, H4 and K4, pin 20. A 250 KHz signal from S1 pin 11 is the clock for the programmable timer section consisting of N5, H5, T5 and K5, pin 2.

INPUT CODE LATCH SYSTEM

Eight input lines from the Logic Board come in on P4 and are pulled up by SIP1 and sent to the two input code latches A3 and B2, one for each microprocessor system. A2, pin 8, becomes a logic high when any of it's inputs are low. This output is connected to pin 11 of the input code latches(A3 and B2). A positive edge at pin 11 causes A3 and B2 to latch the data at their inputs. A2 pin 8 is also connected to the clock inputs of two flip flops, A4 pin 3 and A4 pin 11. When A2 pin 8 goes high, both flip flops are clocked, setting both $\bar{Q}$ outputs low. The $\bar{Q}$ outputs, A4 pin 6 and pin 8, are connected to both of the 6502's active low interrupt request lines, T3 and N1, pin 4. The $\bar{Q}$ outputs of A4 will stay low until the associated 6502 reads its input port therefore clearing the interrupt.

NOTE: DIP switch 3 should remain ON and DIP switch 4 should remain OFF for video games.

DAC PROCESSOR

The DAC processor system (module) consists of N1 (CPU), N2 (data bus driver), K2 (ROM), H2 (RAM), E2 (dual DAC), B2 (input code latch) and half of S2 (decoder). The CPU receives the interrupt from the input latch system (A3, A4) and the NMI (non-maskable interrupt) from S2, pin 10, of the AY processor.

The two jumpers, JP3 and JP4, allow for different types of RAM. For use of HM6116 or 2158A type RAM, JP3 should be connected and JP4 open. If using a 2158B RAM, the opposite applies.

The memory map is split into four 16K boundries by S2, using address lines A14 and A15. These signals are used to select each RAM, ROM, DAC or input port device.

E2 is the Dual Digital to Analog Converter. DAC A is used for a 256 position volume control. It uses +5V DC for a reference voltage and has an op amp (B1 pins 5, 6 and 7)for current to voltage conversion. The output of DAC A at B1 pin 7 should swing between zero and -5V DC, depending on the current converted voltage from DAC A. DAC B's output at B1 pin 8 should swing between zero and +5V DC, depending on the sound being produced. This signal output is capacitively coupled by C13 and sent to the main summer.

AY PROCESSOR

The AY processor system (module) consists of T3 (CPU), S3 (data bus driver), N3 (ROM), K3 (ROM), H3 (RAM), E3, G3, N4, S5 (output ports), B3 (input port), A3 (input code latch), T4 and half of S2 (decoders). The processor, T3, receives its interrupts from its input latch system, A3 and A4, and NMI

(non-maskable interrupt) from the output of the programmable timer, G4 pin 8.

Jumpers JP1 and JP2 at RAM H3, pin 19, allow for different types of RAM. When a HM6116 or 2158A RAM is used, JP1 is connected. When a 2158B is used, JP2 is connected.

The address decoder (T4) uses A13 through A15 to divide the memory map into 8K boundries. Address lines A11 and A12 are also split into 4 by half of S2. This produces eleven active low chip enable signals.

PROGRAMMABLE SOUND GENERATOR

The Programmable Sound Generators, H4 and K4, receive data from N4 (output port) and three control lines from G3 (octal D type latch). Both Programmable Sound Generators use a 2 MHz clock on pin 14 from S1, (synchronous 4-bit counter).

The audio outputs of H4 on pins 15, 17 and 19 are pulled down by R4, R7 and R8 and are summed by R42 through R45 and an op amp H1, pins 1, 2 and 3. The output from H1 pin 1, is capacitively coupled by C23 to the main summer. The audio outputs of K4 on pins 15, 17 and 19, are pulled down by R22, R23 and R24 and summed by R29, R30, R32, R36 and H1 (op amp pins 12, 13 and 14). The output from H1 pin 14 is filtered by two 1.6 KHz low pass filters. The first filter consists of C5, R37, R38 and op amp H1, pins 8, 9 and 10. The second filter consists of C6, R40, R41 and H1 (op amp pins 5, 6 and 7). The output from the second filter is capacitively coupled by C7 to the main summer.

SPEECH

The Speech Synthesizer Chip, E4, receives data from E3 (output port) and three control lines from G3 (output port). The speech chip sends a signal data request on E4, pin 6. The AY processor reads this request through input port B3. The speech chip contains its own 3.12 MHz clock which consists of C1, C2, R1, R2 and XTAL-2. The audio output of the speech chip on pin 19 is pulled up by R3 and is capacitively coupled by C20 to a 160 Hz low pass filter consisiting of C3, R19, R26 and B1. The output at B1 pin 1 is capacitively coupled by C17 to the main summer.

PROGRAMMABLE TIMER

H5 (synchronous 4-bit counter) and K5 form a divide by 256 pre-scaler whose input is 250 KHz and output is 977 Hz. N5, T5 and S5 form a programmable divider whose output at T5 pin 15, can be from 977 Hz to 4 Hz depending upon the value at the output port, S5.

The output of timer T5 causes an NMI to the AY Processor and can be controlled by output G3 using the AND gate G5.

RESET

The Sound Board receives an external reset signal from P3 pin 1. This active low reset signal is pulled up by R34 and sent to G5, pin 1 (2-input AND gate). However, if a manual reset is desired, pushing switch SW2 will reset the processor.

INPUT PORT

Input Port B3 reads the test switch SW1 and two option switches, DIP switches 1 and 2. It also reads four extra inputs from P5 for future expansion. Pressing test switch SW1 will produce a tone.

MAIN SUMMER

The main summer consists of R13 through R17, R20 and B1, pins 12, 13 and 14. B1 pin 14 is the main output from the Sound Board, at P1 pin 2, and will swing plus or minus 5V peak to peak.

IX. THEORY OF OPERATION

SERVICE NOTES